Five Level Modified Cascaded H-Bridge Inverter

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Abstract—This paper presents a cascaded H-bridge multilevel inverter for Electric Vehicle (EV) and Hybrid Electric Vehicle (HEV) application. These new type of inverter are suitable for the high power application due to that the synthesize waveform with better harmonics and output waveform. In this, two H-Bridge inverter are connected in series in which the second H-bridge inverter uses capacitor and this capacitor acts as a DC sources whenever the DC supply is absent the modified PWM techniques is to be developed to reduce the switching losses and also to reduce the total number of switches. To develop the model of the multilevel inverter, a simulation is done by using the MATLAB/SIMULINK software. Here, Sinusoidal Pulse Width Modulation (Phase Opposition Disposition) technique is adopted to obtain a distortion less output for asynchronous motor drives.

Keywords—Multilevel Inverters (MLI), Cascade H-Bridge Inverter, hybrid multilevel inverter, modified cascade h-bridge multilevel inverter, THD, SPWM, APOD, POD.

I. INTRODUCTION

INVERTERS are static power electronics device which is converts dc input voltage to ac output voltage with the desired magnitude and frequency. The output voltage waveforms of ideal inverters should be sinusoidal. But in practically it is square-wave or quasi-square-wave. The multilevel voltage source inverters unique structure allows them to reach medium voltages and high power levels without use of transformers. They are especially suited to high voltage vehicle drives where low output voltage total harmonic distortion (THD) and electromagnetic interference (EMI) are needed. The general function of multilevel inverter is to synthesize a desired voltage from several levels of dc voltages [2].

There are several advantage to multilevel approach as compared to conventional two level approach. The smaller voltage steps lead to the production of higher power quality waveforms and also reduce voltage (dv/dt) stress on the load and the electromagnetic compatibility concerns which ultimately results in output with reduced harmonics.

Another important feature of multilevel converters is that the semiconductors are wired in a series-type connection, which allows operation at higher voltages. However, the series connection is typically made with clamping diodes, which eliminates overvoltage concerns. Furthermore, since the switches are not truly series connected, their switching can be staggered, which reduces the switching frequency and thus the switching losses.

One clear disadvantage of multilevel power conversion is the higher number of semiconductor switches required. It should be pointed out that lower voltage rated switches can be used in multilevel converter and, therefore, the active semiconductor cost is not appreciably increased when compared with the two level cases. However, each active semiconductor added requires associated gate drive circuits and adds further complexity to the converter mechanical layout.

Another disadvantage of multilevel power converters is that the small voltage steps are typically produced by isolated voltage sources or a bank of series capacitors. Isolated voltage sources may not always be readily available, and series capacitors require voltage balancing [2].

II. CASCADE H-BRIDGE

Conventional cascaded multilevel inverters are one of the most important topologies in the family of multilevel and multi-pulse inverters. The cascade topology allows the use of several levels of DC voltages to synthesize a desired AC voltage. The DC levels are considered to be identical since all of them are fuel cells or photovoltaic, batteries, etc. It requires least number of components compared to diode-clamped and flying capacitors type multilevel inverters and no requirement of clamping diodes or voltage balancing capacitors.
Thus a 5 level CHB can be designed by connecting two h-bridge in cascade as shown in fig 1 above. In this one h-bridge generates either polarity i.e. positive and negative and other bridge generates no. of output levels. The resulting output ac voltage swings from to $+V_{dc}$ to $-V_{dc}$ with different levels, and the stair case waveform is nearly sinusoidal, even without filtering. Therefore, the generalized multilevel inverter topology provides a true multilevel structure that can balance each dc voltage level automatically at any number of levels, regardless of active or reactive power conversion, and without any assistance from other circuits. Thus, in principle, it provides a complete multilevel topology that embraces the existing multilevel inverters.

The switching table for 5 level Cascaded H-bridge inverter is as follows:

**Table 1: Switching sequence for 5 level CHB MLI**

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Switches</th>
</tr>
</thead>
<tbody>
<tr>
<td>$+V_{dc}$</td>
<td>1 1 0 0 1 1 0 0</td>
</tr>
<tr>
<td>$+1/2 V_{dc}$</td>
<td>1 0 0 1 0 1 0 1</td>
</tr>
<tr>
<td>0</td>
<td>0 1 0 1 1 0 1 0</td>
</tr>
<tr>
<td>$-1/2 V_{dc}$</td>
<td>0 1 0 1 1 0 0 1</td>
</tr>
<tr>
<td>$-V_{dc}$</td>
<td>0 0 1 1 1 0 0 1</td>
</tr>
</tbody>
</table>

The relation between number of H-bridges and the associated number of output levels can be given as follows:

No. of switches = $(N_{level} - 1) \times 2$

No. of H-Bridge = $(N_{level} - 1) / 2$

**III. MODIFIED H-BRIDGE**

Modified H-bridge multilevel inverter topology separates the output voltage into two parts. One part is named as level generation part and it is responsible for generating levels. The other part is called as polarity generation part and it is responsible for generating the polarity of the output voltage. Positive levels are generated by the level generation part and the output of this part is fed to the polarity generation part in order to generate a complete multilevel output voltage. This will eliminate many of the semiconductor switches which were responsible to generate the output voltage levels in positive and negative polarities.

The main disadvantage of the conventional cascaded H-bridge is that when the voltage level increases, the number of semiconductor switches increases and also the source required increases. In order to overcome this introduced a new topology of cascaded H-bridge. The main advantage of this topology is that the number of switches required is reduced and also the number of sources. Fig 2 shows a modified cascaded h-bridge multilevel inverter using one h-bridge & one power semiconductor switch.

The switching sequence of modified h bridge foe 5 level is as follows:

**Table 2: Switching sequence for modified h-bridge**

<table>
<thead>
<tr>
<th>Voltages</th>
<th>S1</th>
<th>S2</th>
<th>S3</th>
<th>S4</th>
<th>S5</th>
</tr>
</thead>
<tbody>
<tr>
<td>$+V_{dc}$</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>$+1/2 V_{dc}$</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>$-1/2 V_{dc}$</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>$-V_{dc}$</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

The inverter module having a bidirectional switch produces 5-levels of output voltage ($+V_{dc}$, $+1/2 V_{dc}$, 0, $-1/2 V_{dc}$, $-V_{dc}$) by controlling the switches. The H
bridge cell provides the output voltage levels Vdc and -Vdc and other levels are obtained by the auxiliary circuit.

(A) Generation of output levels
1) Level Vdc: S2 is in ON state, connects the load positive terminal to Vdc, and S5 is in ON state, connects the load negative terminal to ground. The other switches are OFF thus the applied voltage to the load terminals is Vdc. Fig. 3 shows the current paths at this stage.[5]

![Fig 3 – Generation of +Vdc voltage level](image)

2) Level Vdc/2: The auxiliary switch, S1 and S5 is ON and the other controlled switches are OFF; the voltage applied to the load terminals is Vdc/2. Fig. 4 shows the current paths at this stage.[5]

![Fig 4 – Generation of +1/2Vdc voltage level](image)

3) Zero output: The two main switches S3 and S5 are ON, short-circuiting the load. All other controlled switches are OFF; the voltage applied to the load terminals is zero. Fig. 5 shows the current paths at this stage.[5]

![Fig 5 – Generation of 0 Vdc voltage level](image)

4) Half-level negative output, Vdc/2: The auxiliary switch, S1 is ON and S4 is ON and the other switches are off.

5) Maximum negative output: S4 is ON and S3 is ON and the other controlled switches are OFF; the voltage applied to the load terminals is -Vdc. Fig. 6 shows the current paths at this stage.[5]

![Fig 6 – Generation of -1/2Vdc voltage level](image)

![Fig 7 – Generation of -Vdc voltage level](image)

IV. SINUSOIDAL PULSE WIDTH MODULATION
Phase Opposition Disposition (POD)

Fig 8 shows POD pulse generation for five level inverter a total of four carrier waves are used. They are arranged in such a manner that all carrier waveforms above zero are in phase and are 180 degree out of phase with those below zero. The converter switches to +Vdc/2 when the sine wave is higher than all carrier waveforms. The converter switches to Vdc/4en the sine is lower than the uppermost carrier waveform and greater than all other carriers. The converter switches to 0 when the sine wave is lower than the two uppermost carrier waveforms and greater than two lowermost carriers. The converter switches to -Vdc/4 when the sine wave is higher than the lower most carrier waveform and lesser than all other carriers. This method uses N – 1 carrier signals to generate N level inverter output voltage. All the carrier signals have the same
amplitude, same frequency and are in phase. In this method triangular carrier wave has been compared with the one sinusoidal reference wave.

V. RESULTS AND DISCUSSION

The model for single leg 5 level multilevel inverter has been simulated in MATLAB/ SIMULINK for resistive load ($R_L = 10$ ohms). The THD analysis was made and found out to be 26.73% for cascade h bridge where as the THD for modified h bridge was found out to be 25.28 and the results are as follows:

Fig 8 - Phase Opposition Disposition SPWM method

Fig.9 Representation of Simulation of five level CHBMLI

Fig.10 current and voltage waveform of five level CHBMLI with R load

Fig.11- FFT spectrum of five level CHBMLI for voltage (with R load)

Fig.12 Representation of simulation of five level MODIFIED CHBMLI with R-load

Fig.13 voltage and current waveform of five level MODIFIED CHBMLI

Fig.14 THD analysis for five level MODIFIED CHBMLI R-load without Filter
VI. CONCLUSION

In this paper, conventional cascade H-bridge and Modified Cascade H-bridge 5 level Multilevel inverter using R-load is simulated using MATLAB simulation. For that SPWM technique(phase opposition and disposition) have been used, from that the THD is comparatively reduced in Modified cascaded multilevel inverter. Modified cascade multilevel inverter requires only 5 switches and two DC source. So, the cost is comparatively reduced for the 5 level and also that there is circuit flexibility, circuit layout and there are no extra clamping diodes or voltage balancing capacitors required. Thus, the modified cascaded H-bridge MLI is beneficial over the other conventional MLI topologies.

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